Evaluation of Property Specification Patterns

Description

Model checking is a computer-assisted verification method. In order to perform verification, the system specification is translated to a temporal-logic formula and the system description is translated to a system model. Formalizing the specification to a temporal-logic formula is hectic for non-experts. To overcome this challenge, pattern-based languages [2, 5, 4] are introduced and successfully applied to the industrial use-cases [6, 3].

The student should provide an overview of the specification patterns (see [1, Section II]), investigate their evaluation aspects and discuss the inferences.

References


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