



Software Engineering Seminar

Property Specification Patterns

Description

Specifying verification properties in a temporal logic (e.g., LTL or CTL) is an error-prone task but required to perform the verification. To ease the specification, property specification patterns have been proposed. For instance, properties could be specified in a structured natural language and automatically translated to a temporal logic. The goal of this topic is to investigate the use of such specification patterns in the literature.

The student should provide an overview of the specification patterns, investigate their use in literature, and finally, classify and discuss the findings.

References

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- [2] Matthew B. Dwyer, George S. Avrunin, and James C. Corbett. Patterns in property specifications for finite-state verification. In *Proceedings of the 21st International Conference on Software Engineering*, ICSE '99, pages 411–420, New York, NY, USA, 1999. ACM.
- [3] Lars Grunske. Specification patterns for probabilistic quality properties. In *Proceedings of the 30th International Conference on Software Engineering*, ICSE '08, pages 31–40, New York, NY, USA, 2008. ACM.
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